

UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)*(Only for new nonprovisional applications under 37 CFR 1.53(b))*

Docket No. EN9-99-082

Total Pages in this Submission
4**TO THE COMMISSIONER FOR PATENTS**

Box Patent Application

Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

Composite Laminate Circuit Structure and Methods of Fabricating

and invented by:

1) Robert M. Japp, 2) Gregory A. Kevern and 3) William J. Rudik

If a **CONTINUATION APPLICATION**, check appropriate box and supply the requisite information:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application no. _____

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Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 22 pages and including the following:
 - a. ☒ Descriptive Title of the Invention
 - b. ☐ Cross References to Related Applications (if applicable)
 - c. ☐ Statement Regarding Federally-sponsored Research/Development (if applicable)
 - d. ☐ Reference to Microfiche Appendix (if applicable)
 - e. ☒ Background of the Invention
 - f. ☒ Brief Summary of the Invention
 - g. ☒ Brief Description of the Drawings (if applicable)
 - h. ☒ Detailed Description
 - i. ☒ Claim(s) as Classified Below
 - j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) (when necessary as prescribed by 35 USC 113)
- a. 4 Number of Sheets
4. ☒ Oath or Declaration
- a. ☒ Newly executed (original or copy) ☐ Unexecuted
- b. Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional application only)
- c. ☒ With Power of Attorney ☐ Without Power of Attorney
- d. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference (usable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche (Appendix)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all must be included)
- a. ☐ Paper Copy
- b. ☐ Computer Readable Copy (identical to computer copy)
- c. ☐ Statement Verifying identical Paper and computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers (cover sheet and document(s))
9. ☐ 37 CFR 3.73(B) Statement (when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☐ 37 CFR 3.73(B) Statement (when there is an assignee)
12. ☐ Preliminary Amendment
13. ☒ Acknowledgement postcard
14. ☒ Certificate of Mailing
☐ First Class Express Mail (Specify Label No.): EL598670482

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Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. ☒ Additional Enclosures (please identify below):

Information Disclosure Statement, Form PTO-1449 and 1 reference

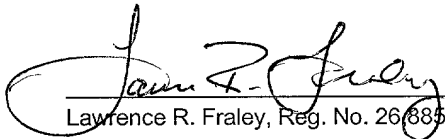
Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	17	- 20 =	0	x \$18.00	\$0.00
Indep Claims	2	- 3 =	0	x \$78.00	\$0.00
Multiple Dependent Claims (check if applicable) <input type="checkbox"/>					\$0.00
BASIC FEE					\$690.00
OTHER FEE (specify purpose)					\$0.00
TOTAL FILING FEE					\$690.00

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- ☒ Charge the amount of \$690.00 as filing fee.
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- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Date: July 25, 2000


Lawrence R. Fraley, Reg. No. 26885 (Signature)

cc:

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09/625135



**APPLICATION
FOR
UNITED STATES LETTERS PATENT**

APPLICANT NAME: Robert M. Japp
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William J. Rudik

TITLE: Composite Laminate Circuit
Structure and Methods of Fabricating

DOCKET NO: EN9-99-082

INTERNATIONAL BUSINESS MACHINES CORPORATION

COMPOSITE LAMINATE CIRCUIT STRUCTURE AND METHODS OF FABRICATING

DESCRIPTION

5

Technical Field

The present invention relates to laminate circuit structures, and more particularly to composite laminate circuit structures constructed from a plurality of modularized
10 circuitized voltage plane subassemblies bonded together. The present invention also relates to a method for fabricating the laminate circuit structures. The present invention provides for planar, fine line external circuit flat lines and does not require an additional adhesive sheet nor glass cloth reinforcement.

15

Background of Invention

A conventional technique of forming a laminate circuit board structures includes forming layers of dielectric material and electrically conducting material to provide multiple layers of circuits and voltage planes. Voltage planes can be either ground plane
20 or power planes, and are sometimes collectively referred to as power planes.

Conventional printed circuit boards are typically constructed from glass cloth prepreg and copper. Normally copper clad laminates (CCL's) are circuitized and then "laid up" with other circuitized cores and additional sticker prepreg to form composites. Once laminated, conventional composite boards are drilled and then plated. While
25 conventional boards can be either tri-plate or strip line constructions, both use conventional prepreg as sticker sheets. Both designs, especially stripline/buried via designs, also usually utilize signal to power plane referencing through the sticker sheet layer, on at least one side of the signal line.

Composites constructed using 2S1P building blocks offer a number of advantages
30 over conventional construction techniques. One of these advantages is testable impedance prior to composite lamination. The impedance is also predominately controlled by the core dielectric. This is a major advantage as core layer dielectrics are not effected by the complex geometries and fill requirements that occur at composite lamination. 2S1P's built with glass cloth free materials facilitate very high circuit density

by allowing very small, laser drilled holes to be made. One very important aspect of using 2S1P's to build high density composite printed circuit boards (PCBs) is the method used to adhere the 2S1P's into a composite board.

5 Prior methods of making 2S1P cores involve drilling or etching clearance holes in bare sheets, e.g., 2 oz., 1 oz. and/or .5 oz., copper and then laminating and fully curing these with conventional prepregs or coated foils to produce a core that could be circuitized forming the signal planes. Likewise, prior OS1P's have been fabricated in similar manners. These methods are difficult to practice due to the problems associated with handling bare copper. 2S1P's can also be made by circuitizing one side of a core
10 with the power pattern then relaminating additional prepreg or coated copper over the circuitized power pattern.

Regardless of the method used to make the 2S1P cores, they must now be stuck together using additional "sticker" materials placed between the 2S1P's and the OS1P's. These additional sticker sheets contribute additional thickness and exacerbate all the
15 problems associated with additional thickness.

More recently, techniques have been provided that provide a relatively inexpensive photolithographic technique of forming a composite laminate structure from individual discrete laminate structures into a composite laminate structure. Along these lines see U.S. applications SN 09/203,945 entitled "Two Signal One Power Plane Circuit
20 Board," SN 09/203,978 entitled "Multi-Layer Organic Chip Carrier Package" and SN 09/204,458(Docket No. EN9-96-122) entitled "Composite Laminate Circuit and Method of Forming the Same," entire disclosures of which are incorporated herein by reference.

Although the structures and methods of these inventions provide significant advances and advantages over current printed wire board (PWB) fabrication methods,
25 there still exists a need for further refinement. Therefore continuing efforts are underway in attempting to provide for even greater advantages.

Summary of Invention

30 The present invention makes possible thinner laminate circuit structures, and therefore making possible higher density PCBs with fewer processing steps. The subject invention teaches new ways to form 2S1P and OS1P components using novel methods, some of which also simplify or solve problems of how to adhere these components together into a

composite, in some cases without the corresponding increase in composite thickness necessitated by the prior art.

In addition, the structures of the present invention do not require glass cloth reinforcement.

5 The present invention improves and simplifies the process for customizing the power planes as well as opening up numerous new possibilities in methods to construct the component cores.

The present invention comprises novel ways for adhering together the subassemblies.

10 The 2S1P and 0S1P structures taught by the present invention each comprise two basic variations. Methods 1, 3, and 5 disclosed below describe how to build 2S1P structures without via holes. 0S1P methods 1 through 4 disclosed below each describe methods of building 0S1P structures each with an option to form conductive holes through the structure. 2S1P methods 1, 3, and 5 and all of the 0S1P methods disclosed
15 below without the conductive hole option exercised are intended for use in composites in which the electrical interconnection scheme will be by conventional composite through hole drilling and plating, thus the conductive pathways will be formed at the composite level. Therefore no need exists for drilling and plating or drilling and filling vias or through holes at the sub component level. 2S1P options 2, 4, and 6 and all of the 0S1P
20 options disclosed below in which the optional through holes have been formed are intended for use in composites in which advanced non-conventional interconnect methods will be employed. Some of these methods include, stacked holes filled with conductive adhesive, stacked dendrite contact, or metal to metal joining.

More particularly, the laminate circuit structure assembly of the present invention
25 comprises at least two modularized circuitized voltage plane subassemblies wherein each of the subassemblies comprise at least two signal planes disposed about an internal voltage plane. Dielectric material is located between the signal and voltage planes. Dielectric is also present on each external surface of each signal plane.

The subassemblies are bonded together into composites with the same dielectric
30 compositions which are used to construct the subassemblies. This is a strategically important part of the invention. For the purposes of physically bonding the 2S1P and 0S1P assemblies no unique adhesives need be used. Additional process steps, (not shown), will be needed to effect electrical interconnection between the vias. For instance,

if stacked vias filled with conductive adhesive is the chosen method of interconnection, then each time a 2S1P via is filled or a 0S1P through hole is filled, they will need to be filled with a conductive adhesive instead of the standard dielectrics as described herein. If stacked dendrites, stacked solder connections or stacked liquid phase metal joining are to be used then filling with the dielectric materials as described is acceptable. These aspects are not discussed at length or detail in this application since alterations necessary to the adopt the described electrical interconnection methods will be apparent to those skilled in the art.

Optionally, an interposer can be located between each of the subassemblies and the cured dielectric wherein the interposer comprises dielectric layers disposed about an internal electrically conductive layer.

The present invention also relates to a method for fabricating a laminate circuit structure assembly. The method comprises providing at least two modularized circuitized voltage plane subassemblies wherein each of the subassemblies comprise at least two signal planes disposed about an internal voltage plane. The signal planes each have an external surface and an internal surface. Dielectric material is located between the signal and voltage planes. At least one via is disposed within each subassembly for providing electrical communication between the signal planes and electrical connection to another of the subassemblies. Dielectric is also provided on each external surface of each signal plane.

An uncured or partially cured curable dielectric composition is located between the subassemblies. The dielectric composition may comprise, various thermosetting resins such as BT epoxy, (bismaleimide-triazine/epoxy blends), difunctional or multifunctional epoxies, cyanate ester resins, polyimide resins, allyated PPO, (polyphenylene ether oxide resins), or cross linked butadiene rubber, or, optionally, various thermoplastic resins such as thermoplastic polyimides, various fluoropolymers, or PPO.

Optionally, an interposer can be located between the subassemblies wherein the interposer comprises dielectric layers are disposed about an internal electrically conductive layer.

The structure is then laminated to cause bonding of the interposer to the subassemblies.

Still other objects and advantages of the present invention will become readily apparent by those skilled in the art from the following detailed description, wherein it is shown and described preferred embodiments of the invention, simply by way of illustration

of the best mode contemplated of carrying out the invention. As will be realized the invention is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects, without departing from the invention. Accordingly, the description is to be regarded as illustrative in nature and not as restrictive.

5

Summary of Drawings

Figure 1 illustrates a 2S1P structure with vias according to the present invention.

Figure 2 illustrates a 0S1P structure with vias according to the present invention.

10 Figure 3 illustrates a structure of the present invention after laminating.

Figure 4 is a flow chart illustrating various alternative sequences that can be followed pursuant to the present invention.

Figure 5 is a flow chart illustrating various alternative sequences that can be followed pursuant to the present invention.

15

Best and Various Modes for Carrying Out Invention

In order to facilitate an understanding of the present invention, reference will be made to the figures wherein the same numerals in different figures refer to the same or corresponding structures. Also in order to facilitate an understanding of the present invention, reference will be made to structures from 2S1P (2 signal plane – 1 power plane) and 0S1P (0 signal plane – 1 power plane) components.

20 Typically, the primary technique for fabricating the above subassembly components comprises applying a sheet of resin, (carried either on copper foil or, on an organic, peelable carrier film such as polyester), to either one or both sides of a 1 oz. or 0.5 oz. double treated copper sheet. During application the resin may or may not be fully cured.

Process flows to fabricate 2S1P and 0S1P subassemblies, covering a number of variations dependent on whether the power plane patterns are to be personalized by etching or drilling, and whether or not they will contain vias will be discussed herein.

30 It should be understood that, in many cases carrier foils made out of alternative metal can be substituted for copper.

Additionally while this specification will largely disclose structures built with resin coated metal foils and resin coated organic carrier foils, it will be apparent to those skilled in the art that the same structures can be formed with slight process alterations using conventional epoxy glass prepregs.

5

Method 1 –

2S1P components with etched power planes and no-vias (fully cured version).

The fully cured version 2S1P components having etched power planes and no vias can be fabricated by laminating two resin coated copper sheets or a coated copper sheet and a copper sheet and fully curing the resin. The resin can be an organic thermoplastic or thermosetting resin. A typical resin coated sheet is available under trade designation RCC from Allied Signal Laminate Systems. The foil layer which is subsequently to become the power plane is preferably double treated. Double treat is copper foil which has had a rough copper oxide/brass adhesion promotion layer applied to both sides.

15 The copper layer which is to become the power plane is patterned using conventional photolithographic techniques, while the copper layer on the other side, which is to become one of the signal layers is protected with a blanket exposed layer of photoresist. The copper used to form the power plane is, most preferably a double treat copper. Single treated copper can be used for the power plane layer but will also require the additional adhesion promotion treatment application described below.

20 The structure is relaminated with another resin coated copper sheet and the resin is fully cured. The two outside signal patterns are then photo patterned and etched.

Additional optional planarization and/or adhesion steps can be carried out. For example, an adhesion promotion step can be employed such as applying an oxide treatment or alternative adhesion promotion treatment, especially if single sided treatment copper were used in forming any of the above power or signal layers. Suitable adhesion promotion treatments include, but are not limited to, copper oxide formation treatments, reduced copper oxide treatment, various silane treatments, tin oxide/silane treatments, and micro etch treatments with Entek or BTA passivation, or the like. One specific example of an acceptable adhesion promotion treatment is Attotech corporation's BONDFILM treatment. The thicknesses of these treatments as recommended by the suppliers of these treatment chemistries are generally acceptable for the purposes of the present invention.

The structure can then be relaminated with another resin coated copper sheet. This layer of dielectric is applied primarily to act as the adhesive at the composite level. This outer layer of dielectric will be partially cured. The surface can be planarized by well known techniques. If desired this resin can be cured, partially cured or remain uncured. If the cure is advanced to only the B-stage, this dielectric can be used later as an adhesive during composite lamination.

The copper carrier is etched or the film carrier, if present, is peeled away.

Method 2 –

2S1P components with etched power planes and vias (fully cured version).

The fully cured version 2S1P components having etched power planes and vias can be fabricated by laminating two resin coated copper coated sheets or a resin coated copper sheet and a copper sheet and fully curing the resin. The foil layer which is subsequently to become the power plane is preferably double treated.

A photoresist is applied using conventional techniques. The pattern on the power plane side is exposed and the signal core side, which is to be protected is blanket exposed. The photoresist on both sides is developed, etched, and stripped on both sides creating the power plane hole pattern using conventional techniques. Some adaptation such as etching frames to prevent curling may be desirable. An adhesion promotion step can be employed such as applying an oxide treatment or alternative adhesion promotion treatment, especially if single sided treatment copper were used in forming any of the above power or signal layers.

The structure is then relaminated with another resin coated copper sheet followed by fully curing the resin. If desired, the outside copper foils are etched down using fluid head etching. Fluid head etching is a technique which is capable of very uniformly etching down the thickness of a large copper surface. This is often done to thin the outside copper layer down so that additional copper can be deposited in the drilled holes, (and on the etched surface), without the differences in thickness between the two being too great.

The desired vias are then drilled and the holes and surfaces are then blanket plated with a conductive metal such as copper. The drilling can be carried out by mechanical or laser drilling. If desired, the holes can optionally be filled with a conductive adhesive, using a conventional hole fill process. The plated holes are then tented over by applying a

photoresist using conventional techniques. Both sides are exposed to the signal patterns. The two outside signal planes are created by developing, etching, and stripping the photoresist using conventional techniques.

5 Additional optional planarization and/or adhesive application steps can be carried out. For instance, an adhesion promotion process can be employed such as applying an oxide to the copper signal plane features.

The structure is then relaminated with another resin coated copper sheet or a resin coated film is applied to fill the via holes. The surface is planarized by well know techniques. If desired, the resin can be cured, partially cured or left uncured.

10 The copper is then etched or the film carrier, if present, is peeled away.

Method 3 –

2S1P components with drilled power planes and no vias (fully cured and relaminated version).

15 The fully cured and relaminated version of 2S1P components having drilled power planes and no vias can be fabricated by laminating two resin coated copper sheets onto a sheet of double treated copper. The copper foils are then etched on both sides of the structure. The power clearance hole pattern is created by drilling through the entire structure.

20 An adhesion promotion step can be employed such as applying an oxide treatment or alternative adhesion promotion treatment. The structure is then relaminated with another pair of resin coated copper sheets thereby filling the holes followed by fully curing the resin. The resin from the second pair of resin coated copper sheets fills the holes.

25 A photoresist is applied using conventional techniques. Both sides are exposed to the signal patterns. The two outside signal planes are created by developing, etching, and stripping the photoresist by using conventional techniques.

30 Additional optional planarization and/or adhesive application steps can be carried out. For example, an adhesion promotion step can be employed such as applying an oxide. The structure can then be relaminated with another resin coated copper sheet or a resin coated film can be applied. If desired, the resin can be cured, partially cured or left uncured. If the cure is advanced to only the B-stage, this dielectric can be used later as an adhesive during composite lamination. The copper is etched or the film carrier, if present is peeled away.

Method 4 –

2S1P with drilled power planes and vias (fully cured and relaminated version).

5 The fully cured and relaminated version of 2S1P components having drilled power planes and vias can be fabricated by laminating two resin coated copper sheets onto a sheet of double treated copper. The copper foils are then etched off both sides of the structure. The power clearance hole pattern is created by drilling through the entire structure. An adhesion promotion step can be employed such as applying an oxide treatment or alternative adhesion promotion treatment. The structure is then relaminated with another resin coated
10 copper sheet thereby filling the clearance holes. The resin is then fully cured.

If needed, the outside foils can be etched down such as by fluid head etching.

Vias are then drilled in the structure followed by blanket plating a conductive metal in the holes and over the surface. A photoresist is applied using conventional techniques. Both sides are exposed to the signal patterns. The two outside signal planes are created by
15 developing, etching, and stripping the photoresist by using conventional techniques.

Additional optional planarization and/or adhesive application steps can be carried out. For example, an adhesion promotion step can be employed such as applying an oxide. The structure can then be relaminated with another resin coated copper sheet or a resin coated film can be applied to fill the via holes. If desired, the resin can be cured, partially
20 cured or remain uncured. If the cure is advanced to only the B-stage, this dielectric can be used later as an adhesive during composite lamination. The copper is then etched or the film carrier, if present, is peeled away. The surface is planarized by well known techniques to remove excess resin.

In addition, an adhesion promotion step can be employed at this stage such as
25 applying an oxide treatment or alternative adhesion promotion treatment.

Method 5 –

2S1P with drilled power planes and no vias (non-fully cured and relaminated version).

30 The non-fully cured and relaminated version of 2S1P components having drilled power planes and no vias can be fabricated by applying two resin coated films to both sides of a sheet of double treated copper. The cure is not advanced at this stage. The copper foils are etched off both sides of the structure or the carrier film is peeled away. The power clearance hole pattern is created by drilling through the entire structure. An

adhesion promotion step can be employed such as applying an oxide treatment or alternative adhesion promotion treatment. The structure is then relaminated with copper foil on both sides and the uncured resin is reflowed thereby filling the holes. Optionally, instead of copper an additional resin coated copper sheet can be used to assist in hole fill. If
5 desired, the outside copper foils are etched down using fluid head etching. Fluid head etching is a technique which is capable of very uniformly etching down the thickness of a large copper surface. This is often done to thin the outside copper layer down so that additional copper can be deposited in the drilled holes, (and on the etched surface), without the differences in thickness between the two being too great. The resin is then
10 fully cured. A photoresist is applied using conventional techniques. Both sides are exposed to the signal patterns. The two outside signal planes are created by developing, etching, and stripping the photoresist by using conventional techniques.

Additional optional adhesive application steps can be carried out. For example, the structure can be relaminated with a resin coated copper sheet or a resin coated film can be
15 applied. The cure is not advanced. If the cure is advanced to only the B-stage, this dielectric can be used later as an adhesive during composite lamination. The copper is then etched or the film carrier, if present, is peeled away.

Method 6 –

20 2S1P with drilled power planes and vias (not fully cured after relamination version).

The non-fully cured after relamination version of 2S1P components having drilled power and vias can be fabricated by applying two resin coated films to both sides of a sheet of double treated copper. The cure is not advanced at this stage. The copper foil is etched off both sides or the carrier film (typically Mylar) is peeled off both sides. The power
25 clearance hole pattern is created by drilling through the entire structure. An adhesion promotion step can be employed such as applying an oxide treatment or alternative adhesion promotion treatment. The structure is then relaminated with another copper foil on both sides and the uncured resin is caused to reflow filling the holes. Optionally, resin coated copper sheets can be applied instead of plain treated copper to assist in the hole fill. The
30 resin is then fully cured in this lamination step. The outside foils are etched down, typically using a fluid head etch.

The vias are then drilled followed by blanket plating the holes and surfaces with a conductive metal such as copper. Optionally, the vias can be filled with a conductive

adhesive. A photoresist is applied using conventional techniques. Both sides are exposed to the signal patterns. The two outside signal planes are created by developing, etching, and stripping the photoresist by using conventional techniques.

Additional optional planarization and/or adhesive application steps can be carried out. For example, an adhesion promotion step can be employed such as applying an oxide. The structure can then be relaminated with another resin coated copper sheet or a resin coated film can be applied to fill the via holes. The planarization can be carried out by well known techniques. If desired, the resin can be cured, partially cured or remain uncured. If the cure is advanced to only the B-stage, this dielectric can be used later as an adhesive during composite lamination. The copper is etched or the film carrier, if present, is peeled away.

In addition, an adhesion promotion step can be employed at this stage such as applying an oxide treatment or alternative adhesion promotion treatment.

Alternatively, any of the above processes can be modified such as by performing the signal and/or power plane circuitization steps using additive circuitization as is well known in the art.

Method 7 –

OS1P with etched power planes (fully cured version).

OS1P components having etched power planes can be fabricated by laminating two resin coated copper sheets or an resin coated copper sheet and a copper sheet and fully curing the resin. The foil layer which is subsequently to become the power plane is preferably double treated. The power pattern is then etched on one side while protecting the foil on the other side. An adaptation such as etching frames to prevent curling may be desirable. The structure is relaminated with another resin coated copper sheet on one side only and the resin is fully cured.

The outside copper layers are etched or the film carrier is peeled away by conventional techniques. Optionally, holes can be drilled by mechanical or laser drilling. Also the surface and holes, if present, can be blanket seeded and plated with a conductive metal using conventional techniques. The plated holes, if present, can optionally be tented over by applying a photoresist using conventional techniques. Both sides are exposed to the signal patterns. The two outside signal planes are created by developing, etching, and stripping the photoresist using conventional techniques.

Additional optional adhesion promotion steps can be carried out. For instance, an adhesion promotion process can be employed such as applying an oxide to the copper signal plane features. If desired, the holes can optionally be filled with a conductive adhesive, using a conventional hole fill process and excess adhesive removed.

5 Additional optional adhesive application steps can be carried out. For example, the structure can be relaminated with another resin coated copper sheet or a resin coated film can be applied. The cure is not advanced. The copper is etched or the film carrier, if present, is peeled away.

The copper is then etched or the film carrier, if present, is peeled away. The surface
10 is planarized by well known techniques to remove excess resin.

In addition, an adhesion promotion step can be employed at this stage such as applying an oxide treatment or alternative adhesion promotion treatment.

Method 8 –

15 OS1P with drilled power planes (fully cured version).

The fully cured version of OS1P components having drilled power planes can be fabricated by applying two resin coated copper sheets to both sides of a sheet of double treated copper. The cure of the resin is not advanced at this stage. The copper foils are etched or the carrier film (e.g., Mylar) is peeled off both sides of the structure. The power
20 clearance hole pattern is created by drilling through the entire structure. Additional optional adhesive promotion steps can be carried out. For instance, an adhesion promotion process can be employed such as applying an oxide.

The structure is relaminated with additional resin coated copper sheets or resin coated films whereby the resin fills the holes. The resin is then fully cured.

25 The two outside copper foils are etched or the two carrier films are peeled off.

Optionally, holes can be drilled by mechanical or laser drilling. Also the surface and holes, if present, can be blanket seeded and plated with a conductive metal using conventional techniques. The plated holes, if present, can optionally be tented over by applying a photoresist using conventional techniques. Both sides are exposed to the signal
30 patterns. The two outside signal planes are created by developing, etching, and stripping the photoresist using conventional techniques.

Additional optional adhesive promotion steps can be carried out. For instance, an adhesion promotion process can be employed such as applying an oxide to the copper signal

plane features. If desired, the holes can optionally be filled with a conductive adhesive, using a conventional hole fill process and excess adhesive removed.

Additional optional adhesive application steps can be carried out. For example, the structure can be relaminated with another resin coated copper sheet or a resin coated copper film can be applied. The cure of the resin is not advanced. The copper is etched or the film carrier, if present, is peeled away. The copper is then etched or the film carrier, if present, is peeled away. The surface is planarized by well known techniques to remove excess resin.

In addition, an adhesion promotion step can be employed at this stage such as applying an oxide treatment or alternative adhesion promotion treatment.

Method 9 –

0S1P with drilled power planes (non-fully cured after first lamination and then fully cured after second lamination version).

The version of 0S1P having drilled power planes and being non-fully cured after the first lamination but fully cured after the second lamination can be fabricated by laminating two resin coated copper coated sheets or applying two resin coated copper films to both sides of a sheet of double treated copper. The cure of the resin is not advanced at this stage. The copper foils are etched off both sides, or the carrier film is peeled off. The power clearance hole pattern is created by drilling through the entire structure. In addition, an adhesion promotion step can be employed at this stage such as applying an oxide treatment or alternative adhesion promotion treatment.

The structure is relaminated with copper, shiny copper foil or a release sheet on both sides of the copper foil. Optionally, resin coated copper sheets can be applied instead of plain treated copper to assist in the hole fill. The uncured resin is reflowed filling the holes followed by curing the resin. The copper is etched or the shiny copper is peeled off or the release film is peeled off.

Optionally, holes can be drilled by mechanical or laser drilling. Also the surface and holes, if present, can be blanket seeded and plated with a conductive metal using conventional techniques. The plated holes, if present, can optionally be tented over by applying a photoresist using conventional techniques. Both sides are exposed to the signal patterns. The two outside signal planes are created by developing, etching, and stripping the photoresist using conventional techniques.

Additional optional adhesive promotion steps can be carried out. For instance, an adhesion promotion process can be employed such as applying an oxide to the copper signal plane features. If desired, the holes can optionally be filled with a conductive adhesive, using a conventional hole fill process and excess adhesive removed.

5 Additional optional adhesive application steps can be carried out. For example, the structure can be relaminated with another resin coated copper sheet or a resin coated copper film can be applied. The cure of the resin is not advanced. The copper is etched or the film carrier, if present, is peeled away. The surface is planarized by well known techniques to remove excess resin.

10 In addition, an adhesion promotion step can be employed at this stage such as applying an oxide treatment or alternative adhesion promotion treatment.

Method 10 –

15 OS1P with drilled power planes (non-fully cured version).

The non-fully cured version of OS1P components drilled power planes can be fabricated by laminating two resin coated copper sheets or by applying two resin coated copper films to both sides of a sheet of double treated copper. The cure of the resin is not advanced.

20 The copper foils are etched off both sides or the carrier film is peeled off. The power clearance hole pattern is created by drilling through the entire structure. In addition, an adhesion promotion step can be employed at this stage such as applying an oxide treatment or alternative adhesion promotion treatment.

25 The structure is relaminated with copper, shiny copper foil or a release film, such as Teflon. The uncured resin is reflowed filling the holes. Optionally, resin coated copper sheets can be applied instead of plain treated copper to assist in the hole fill. The resin cure is not advanced. The copper foil is etched or the shiny copper or release film is peeled off.

30 Optionally, holes can be drilled by mechanical or laser drilling. Also the surface and holes, if present, can be blanket seeded and plated with a conductive metal using conventional techniques. The plated holes, if present, can optionally be tented over by applying a photoresist using conventional techniques. Both sides are exposed to the signal

patterns. The two outside signal planes are created by developing, etching, and stripping the photoresist using conventional techniques.

Additional optional adhesive promotion steps can be carried out. For instance, an adhesion promotion process can be employed such as applying an oxide to the copper signal plane features. If desired, the holes can optionally be filled with a conductive adhesive, using a conventional hole fill process and excess adhesive removed.

Additional optional adhesive application steps can be carried out. For example, the structure can be relaminated with another resin coated copper coated sheet or a resin coated copper film can be applied. The cure of the resin is not advanced. The copper is etched or the film carrier, if present, is peeled away. The surface is planarized by well known techniques to remove excess resin.

In addition, an adhesion promotion step can be employed at this stage such as applying an oxide treatment or alternative adhesion promotion treatment.

It is understood that various modifications of any of the above methods can be employed if and when desired. For instance, instead of using a double treated double sheets for fabricating power planes, a single treated foil can be used. However, such would require an additional adhesion promotion step at an appropriate stage. Likewise, it may be desirable especially from a cost effectiveness standpoint to employ conventional hole fill techniques for the through vias instead of the relamination with a resin coated copper sheet. Also, etch power plane techniques can be used in producing 2S2P and 0S2P cross sections. These core structures offer certain advantages in constructing stripline cross sections, including improved capacitance, power distribution and thickness reduction.

Furthermore, if desired hybrid structures such as performing the above resin coated copper sheet or film carried resin processing can be formed on conventional glass containing prepreg cores, thereby potentially reducing cost by both material and processing savings. This would apply particularly to conventional double sided etched cores used as the starting point for 2S2P and 0S2P structures.

In any event, the above described 2S1Ps and if desired 0S1Ps can be laid up next to each other in various combinations to form for example tri-plate or stripline structure provided that at least one of adjoining subassemblies contains uncured resin on its outside surface to act as an adhesive bonding layer. If desired, all of the cores can have the

uncured or B-staged sticker coating or only every other core needs to have an adhesive layer thereon.

According to the present invention, the dielectric compositions employed as the adhesive comprise the following ingredients and in the following relative amounts:

5 One important consideration in dielectric or adhesive selection is whether or not material will be expected to withstand exposure to water, (during photolithographic processing and etching), while in the B-staged or uncured state. Some materials are capable of this while such exposure causes irreversible detrimental changes in others, such as inability to be fully cured at a later time. Thus selection of an
10 appropriate dielectric for the intended build methodology is important. The BT/epoxy blends, various epoxies and cyanate esters, are examples of materials which can tolerate moisture exposure while B-staged and still be successfully fully cured later. The APPE and most polyimides are examples of materials that are not water tolerant in the B-stage. Thermoplastic materials in general are water tolerant. Materials that are not water
15 tolerant can be used in many of the build methodologies described earlier, but not the methodologies which require relamination after exposure to water.

Typical acceptable BT formulations include, but are not limited to, BT/epoxies comprising about 4% bismaleimide polyimide, about 20 % brominated difunctional epoxy, about 5% tetrafunctional epoxy, about 20% highly brominated epoxy, and about
20 30% cyanate ester resin with about .03% zinc octuate added as catalyst. Other acceptable commercially available BT/epoxies include the Mitsubishi 830 and 832 BT/epoxy formulations. These materials are water tolerant in the B-stage.

Acceptable epoxies include most of those that do not contain DICY, (dicyandiamide), and include, but are not limited to, Ciba 8123, and Shell 2414 both of
25 which use approximately .15% 2-methylimidazole as the catalyst. These materials are water tolerant in the B-stage.

Acceptable cyanate esters include N-7000 sold by Nelco. This material is water tolerant in the B-stage.

Acceptable APPE materials include S-2100, S-2122, S-3100 and S3122 and the
30 coated copper version of these PC-5100, made by Asahi Chemical and equivalent products. Also acceptable is the polymer coated film APPE material made by Asahi. These materials are not water tolerant in the B-stage.

The thickness of the coated material used depends on many factors including the weight of the power plane, whether the holes are etched or drilled, what the desired finished board electrical impedance is, and whether the subject dielectric layer is being used to fill power plane holes, signal planes vias, or simply as the adhesive layer. In general thickness of about 1.5 to about 2.0 mils applied to either side of the etched power plane copper are sufficient to fill the holes. The thickness required to fill holes drilled in power planes and the adjacent dielectric depends on whether the adjacent dielectric was B-staged or fully cured when it was applied, but generally about 2.0 to about 2.5 mils applied to both sides of the drilled power plane assembly will fill the drilled holes. Dielectric layers whose job is to act as the adhesive layer at composite lamination can be between about 0.25 and about 1.0 mils thick depending on whether the outside surfaces of every component are coated or if only every other component is coated.

The lamination of the structure is typically carried out at temperatures of about 100° to about 200°C for about 15 minutes to about 90 minutes and at a pressure of about 100 psi to about 500 psi.

It has been determined according to the present invention that the uncured or partially cured compositions employed can be exposed to the liquid processing chemicals, dried, subsequently reflowed or reflowed and then cured thereby enabling one coating pass to perform multiple functions as contrasted to prior techniques which required several coating passes. These functions include, stiffening and improving the handling of thin copper sheets, flowing to fill holes and planarizing, and reflowing to adhere layers of a composite together. The compositions employed pursuant to the present invention exhibit a combination of having low moisture absorption, low chemical interaction with moisture, being slow curing over a wide temperature range between flow onset and cure, and has particular flow characteristics. This combination of characteristics makes it possible to achieve the various objectives according to the present invention.

Figure 1 illustrates a 2SIP subassembly with vias after planarization wherein, numeral 1 represents first dielectric layers and numeral 2 represents a power plane. Numeral 3 represents second dielectric layers. Numeral 4 represents signal lines and 5 represents signal via. Numeral 6 represents power connected via and 7 represents a conductive adhesive filled via. Numeral 8 represents drilled or etched clearance hole. The subassembly of Figure 1 can be fabricated by Methods 2, 4 and 6.

Figure 2 illustrates a 0SIP subassembly with vias wherein numeral 11 represents a B-staged dielectric adhesive and 12 a power or ground plane. Numeral 13 represents conductive adhesive filled via and 14, a resin filled clearance hole.

5 Figure 3 illustrates, a structure of the present invention after laminating wherein numeral 20 represents 2SIP subassemblies according to Figure 1 and 21 represents 0SIP subassembly according to Figure 2.

The foregoing description of the invention illustrates and describes the present invention. Additionally, the disclosure shows and describes only the preferred embodiments of the invention but, as mentioned above, it is to be understood that the invention is capable of use in various other combinations, modifications, and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein, commensurate with the above teachings and/or the skill or knowledge of the relevant art. The embodiments described hereinabove are further intended to explain best modes known of practicing the invention and to enable others skilled in the art to utilize the invention in such, or other, embodiments and with the various modifications required by the particular applications or uses of the invention.

10 Accordingly, the description is not intended to limit the invention to the form disclosed herein. Also, it is intended that the appended claims be construed to include alternative embodiments.

20

CLAIMS

What is claimed is:

- 1 1. A laminate circuit structure assembly comprising at least two modularized
2 circuitized voltage plane subassemblies wherein each of the subassemblies comprise at least
3 two signal planes having an external and internal surface disposed about an internal voltage
4 plane; dielectric between the signal and voltage planes; and dielectric on each external
5 surface of each signal plane; and wherein the subassemblies are bonded together with a
6 cured dielectric from a composition comprising the same dielectric used in said
7 subassemblies.
- 1 2. The laminate circuit structure of Claim 1 which further includes an
2 interposer located between the subassemblies wherein the interposer located between the
3 subassemblies comprises dielectric layers disposed about an internal electrically conductive
4 layer.
- 1 3. The laminate circuit structure of Claim 1 wherein the dielectric of at least
2 one of the surfaces that is bonded is from said composition.
- 1 4. The laminated circuit structure of Claim 1 wherein vias are disposed within
2 each subassembly for providing electrical communication between signal planes and
3 electrical connection to another subassembly.
- 1 5. The laminate circuit structure assembly of Claim 4 wherein the vias through
2 the signal planes are plated with a conductive metal.

1 6. The laminate circuit structure assembly of Claim 2 wherein the internal
2 electrically conductive layer of the interposer is copper.

1 7. The laminate circuit structure assembly of Claim 2 wherein the interposer is
2 about 3 mils to about 10 mils thick.

1 8. A method for fabricating a laminate circuit structure assembly which
2 comprises providing at least two modularized circuitized voltage plane subassemblies
3 wherein each of the subassemblies comprise at least two signal planes having an external
4 and internal surface disposed about an internal voltage plane; providing dielectric between
5 the signal and voltage planes; and providing dielectric on each external surface of each
6 signal plane; and providing a non-cured or partially cured curable dielectric composition
7 between the subassemblies wherein the dielectric composition comprises, the same
8 dielectric used in said subassemblies, aligning the subassemblies, and then laminating to
9 cause bonding of the subassemblies.

1 9. The method of Claim 8 which further comprises locating an interposer
2 between the subassemblies wherein the interposer comprises dielectric layers disposed about
3 an internal electrically conductive layer.

1 10. The method of Claim 9 wherein dielectric of at least one of the surfaces that
2 is to be bonded is from said dielectric composition.

1 11. The method of Claim 8 wherein vias are disposed within each subassembly
2 for providing electrical communication between signal planes and electrical connection to
3 another subassembly.

1 12. The method of Claim 11 wherein the vias through the signal planes are
2 plated with a conductive metal.

1 13. The method of claim 11 wherein the vias are filled with conductive adhesive.

1 14. The method of Claim 9 wherein the internal electricity conductive layer of
2 the interposer is copper.

1 15. The method of Claim 9 wherein the interposer is about 3 to about 10 mils
2 thick.

1 16. The method of Claim 8 which comprises providing top and bottom
2 circuit layers on top and bottom external surfaces of the assembly.

1 17. The method of Claim 8 wherein the laminating is carried out at about 100
2 to about 200°C, for about 15 minutes to about 90 minutes, and at a pressure of about 100
3 to about 500 psi.

COMPOSITE LAMINATE CIRCUIT STRUCTURE AND METHODS OF FABRICATING

5

ABSTRACT OF DISCLOSURE

10 A laminate circuit structure assembly is provided that comprises at least two modularized circuitized voltage plane subassemblies; optionally an interposer located between each of the subassemblies and wherein the subassemblies and interposer, if present, are bonded together with a cured dielectric coating. The interposer comprises dielectric layers disposed about an internal electrically conductive layer.

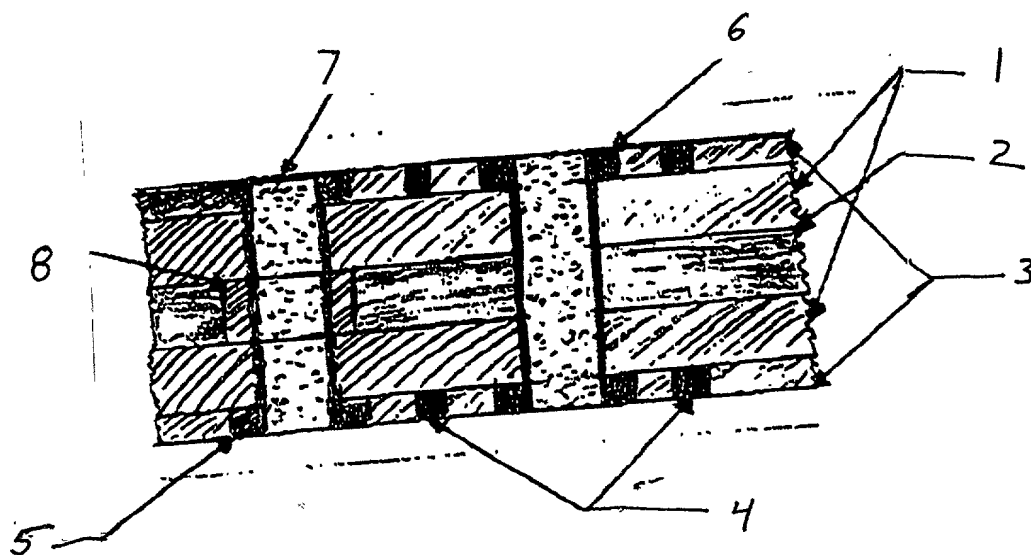


FIGURE 1

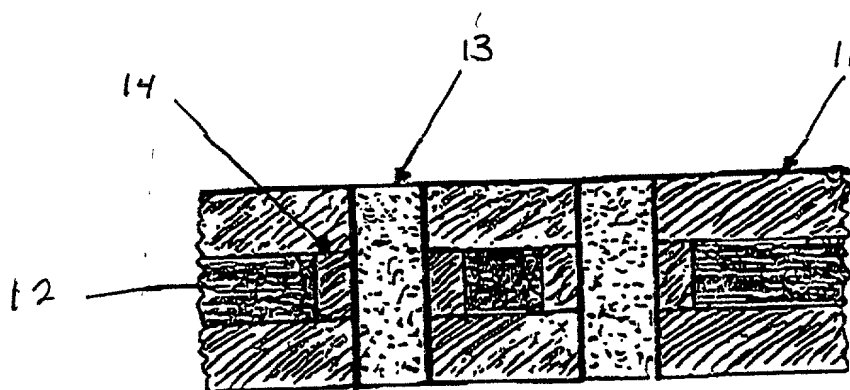


FIGURE 2

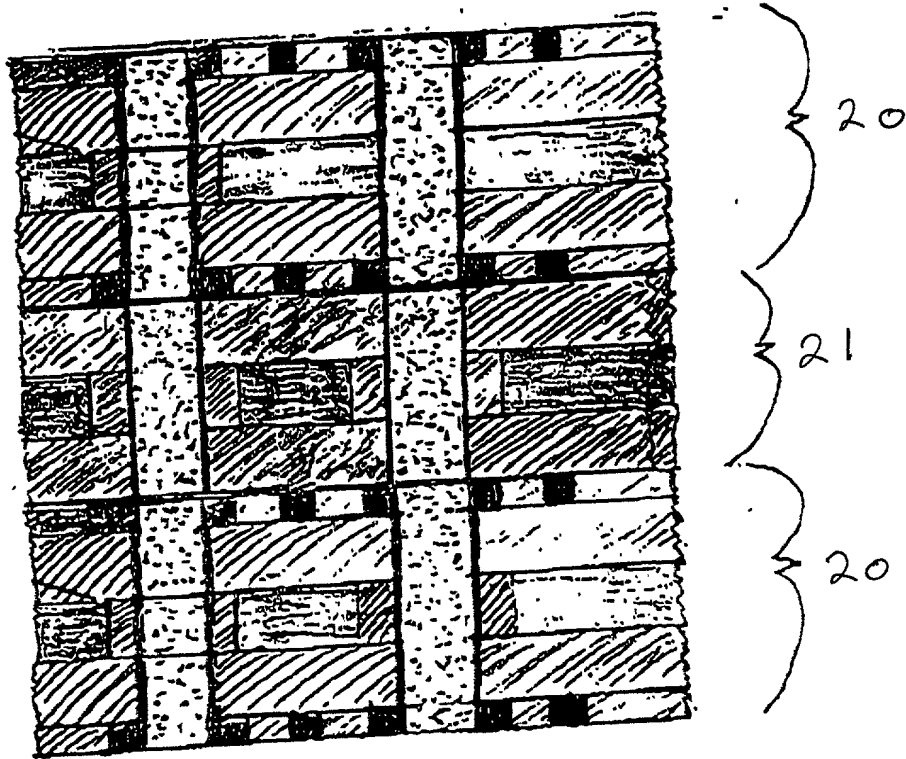


FIGURE 3

2S1P With Drilled Powers and Vias

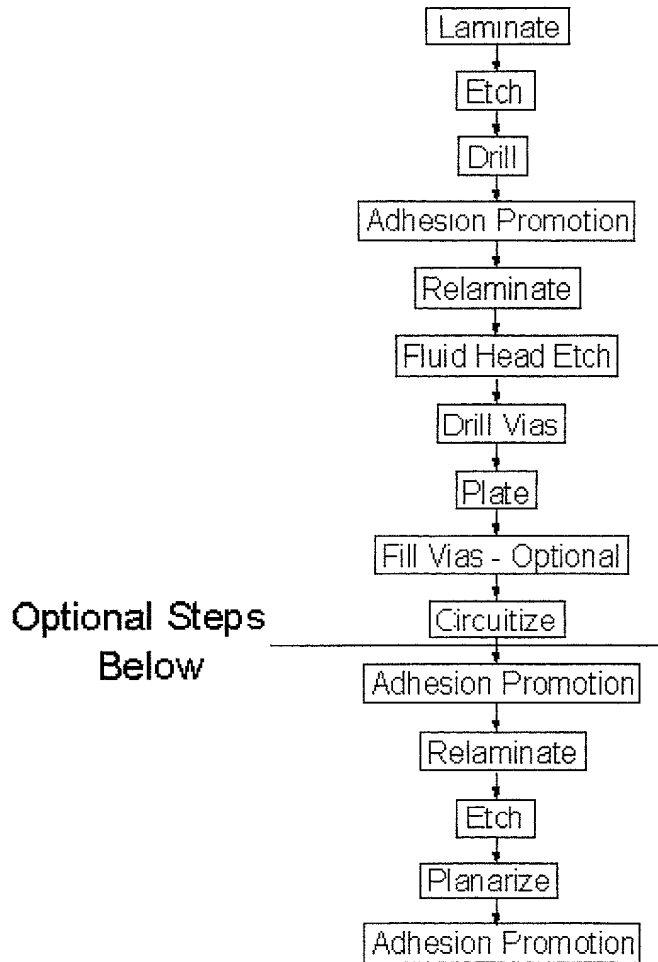


FIGURE 4

OS1P with Drilled Powers

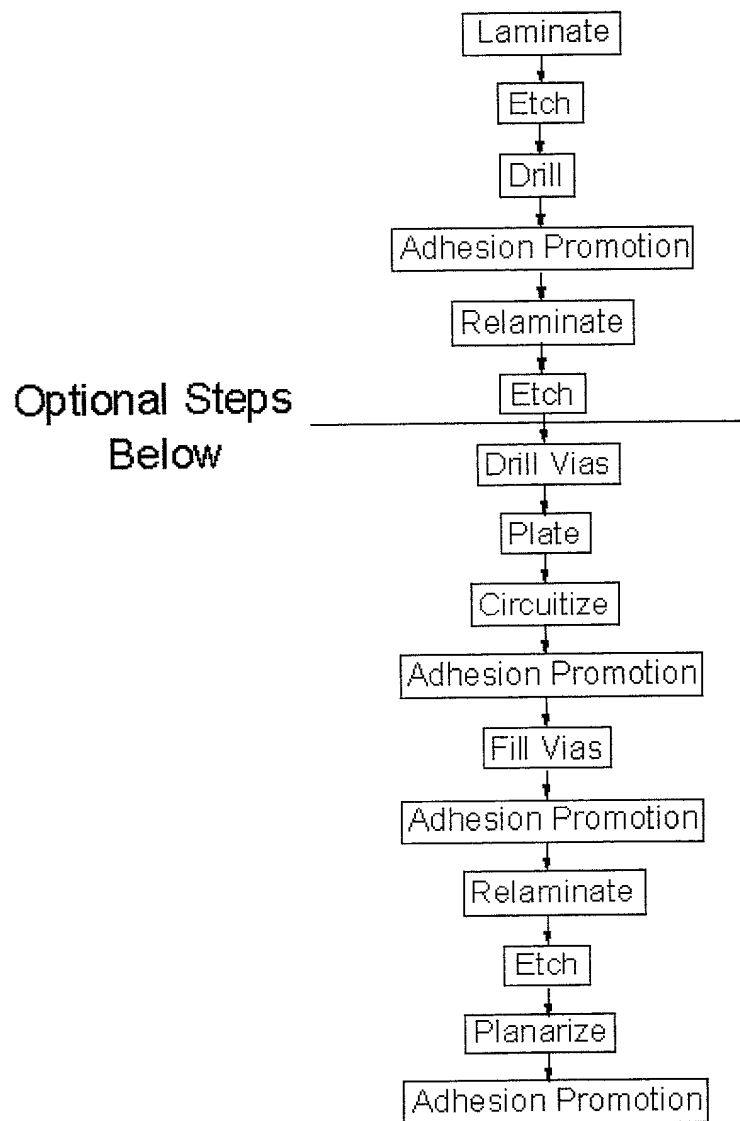


FIGURE 5

DECLARATION FOR PATENT APPLICATION

English Language Declaration

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Composite Laminate Circuit Structure and Methods of Fabricating

the specification of which
(check one)

- ☒ is attached hereto.
☐ was filed on _____, as United States Patent Application Serial No. or PCT International Application Number _____, and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 CFR § 1.56(a).

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate listed below, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

			Priority Claimed	
_____ (Application No.)	_____ (Country)	_____ (Day/Month/Year Filed)	[] YES	[] NO
_____ (Application No.)	_____ (Country)	_____ (Day/Month/Year Filed)	[] YES	[] NO
_____ (Application No.)	_____ (Country)	_____ (Day/Month/Year Filed)	[] YES	[] NO

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

_____ (Application Serial No.)	_____ (Filing Date)
_____ (Application Serial No.)	_____ (Filing Date)
_____ (Application Serial No.)	_____ (Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by 35 U.S.C. § 112, first paragraph, I acknowledge the duty to disclose material information as defined in 37 CFR § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

_____ (Application Serial No.)	_____ (U.S. Filing Date)	_____ (Status) (patented, pending, abandoned)
_____ (Application Serial No.)	_____ (U.S. Filing Date)	_____ (Status) (patented, pending, abandoned)
_____ (Application Serial No.)	_____ (U.S. Filing Date)	_____ (Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: *(list name and registration number)*

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Citizenship _____
Post Office Address _____

Full name of fifth joint inventor (if any) _____

Inventor's Signature _____ Date _____
Residence Address _____
Citizenship _____
Post Office Address _____

Full name of sixth joint inventor (if any) _____

Inventor's Signature _____ Date _____
Residence Address _____
Citizenship _____
Post Office Address _____

Full name of seventh joint inventor (if any) _____

Inventor's Signature _____ Date _____
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Citizenship _____
Post Office Address _____